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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,269	09/19/2003	Joseph Patino	CE11663JDP	6045

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EXAMINER	
YACOB, SISAY	

ART UNIT	PAPER NUMBER
2635	

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Please find below and/or attached an Office communication concerning this application or proceeding.

H'D

Office Action Summary	Application No.	Applicant(s)	
	10/667,269	PATINO ET AL.	
	Examiner	Art Unit	
	Sisay Yacob	2635	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1 The application of Patino et al., "Keypad array having reduced number of input/outputs and method for generating same" filed on September 19, 2003 has been examined.

Claims 1- 14 are pending.

Claim Rejections - 35 USC § 102

2 The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3 Claims 1-7 and 11-14 are rejected under 35 U.S.C. 102(b) as being anticipated by US patent of Thus (6,326,906).

4 As to claim 1, Thus discloses a method of generating an array having a reduced number of input/outputs (See figures 2-4) comprising the steps of for each array row input/output (Col. 3, lines 12-40), grouping at least one set of rows in which the set of rows is coupled to the array row input/output (Items R1-3 of figure 2), and for each combination of the array row input/outputs, selectively

coupling non-set rows to the array row input/outputs that comprise the combination (Items 3-5 of figure 2), wherein at least a portion of a number of rows for the array is equal to the number of rows in each set of rows multiplied by the number of input/outputs coupled to the array row input/outputs plus the number of non-set rows coupled to the array input/output combinations (Col. 3, lines 12-40; See figures 2-3).

5 As to claim 2, the method according to claim 1, further, Thus discloses each set of rows includes a first row and a second row (See figure 4), the method comprises the step of positioning at least one passive element between the second row and the array row input/output (Col. 2, lines 54-60; Col. 3, lines 27-33; Items 3-5 of figures 2; Items d1-9 of figures 3).

6 As to claim 3, the method according to claim 2, further, Thus discloses wherein the passive element is a diode (Col. 2, lines 54-60; Col. 3, lines 27-33; Items 3-5 of figures 2; Items d1-9 of figures 3).

7 As to claim 4, the method according to claim 1, further, Thus discloses the step of positioning a passive element between each non-set row and each of the array row input/outputs that comprise the combination (Items P0-3 and items 6-9 of figures 4).

8 As to claim 5, the method according to claim 4, further, Thus discloses the passive element is a diode (Items 6-9 of figures 4).

9 As to claim 6, the method according to claim 1, further, Thus discloses the array further has a number of keys, switches (Col. 2, lines 28-30) and columns (Col. 2, lines 23-27) and the keys are coupled to the switches, wherein the switches are coupled to the rows in the set of rows (Items R1-3 of figures 2-3), the non-set rows (Items 3-5 and d1-9 of figures 2-3) and columns (C1-3 of figures 2-3).

10 As to claim 7, the method according to claim 6, further, Thus discloses the step of, in response to at least one of the keys being activated, selectively transitioning the rows in the set of rows and the non-set rows between low and high states and transitioning the columns between low and high input states to determine which key has been activated (Col. 2, lines 54-67; Col. 3, lines 1-25).

11 As to claim 11, the array according to claim 1, further, Thus discloses a passive element positioned between each said non-set row and each of said array row input/outputs that comprise said combination (Items P0-3 and items 6-9 of figures 4).

12 As to claim 12, the array according to claim 11, further, Thus discloses the passive element is a diode (Items 6-9 of figures 4).

13 As to claim 13, the array according to claim 1, further, Thus discloses at least one switch (Col. 2, lines 28-30), wherein the switches are associated with corresponding keys and the switches are coupled to the rows in the set of rows, the non-set rows and the columns (Col. 2, lines 54-67; Col. 3, lines 1-25).

14 As to claim 14, the array according to claim 13, further, Thus discloses the array is part of a system having a processor (Item 2 of figures 2-4) and the array input/outputs are coupled to the processor (Col. 2, lines 14-16, 27-32), wherein the processor, in response to at least one of the key being activated, selectively transitions the rows in the set of rows and the non-set rows between low and high states and the columns between input low and high states to determine which the key has been activated (Col. 2, lines 54-67; Col. 3, lines 1-11).

Rejections - 35 USC § 103

15 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

16 Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent of Thus (6,326,906) in view of US patent of Schnizlein et al., (6,424,274).

17 As to claim 8, Thus discloses an array having a reduced number of input/outputs (Col. 3, lines 12-40; See figures 2-3) comprising at least one column (Item C1-3 of figures 2-3; Items P0-3 of figure 4), and at least one set of rows for each array row input/output (Items R1-3 of figures 2-3), wherein the set of rows are coupled to the array row input/outputs (Items R1, 1, 2, 3 of figures 2-3 Item C1-3 of figures 2-3) and a predetermined number of said array row input/outputs form combinations, wherein if non-set rows are added to the array (Items 3, *, 0, # and d1-3 of figures 2-3), said non-set rows are coupled to the array row input/outputs that comprise a combinations (Items P0-3 and items 6-9 of figures 4), however, Thus does not expressly discloses the portion of a number of rows for the array is equal to the number of rows in each set of rows multiplied by the number of array row input/outputs plus the number of non-set

rows coupled to the array row input/output combinations. In the same field of endeavor, Keypad scanning with few input/outputs, Schnizlein et al., discloses an array having a reduced number of input/outputs (Col. 3, lines 54-67; Col. 4, lines 1-14).

It would have been obvious, to one ordinary skill in the art, at the time of the invention, to modify the array having a reduced number of input/outputs of Thus, by incorporating the array having a reduced number of input/outputs that comprises a number of rows that are coupled to row input/output, as discloses by Schnizlein et al., in order to have the array having a reduced number of input/outputs comprising a combinations at least a portion of a number of rows for the array is equal to the number of rows in each set of rows multiplied by the number of array row input/outputs plus the number of non-set rows coupled to the array row input/output combinations, because Thus discloses the array having a reduced number of input/outputs that comprises an array rows coupled to input/outputs and the array may accommodate a large number of keys (Col. 3, lines 26-40) and Schnizlein et al., discloses the array having a reduced number of input/outputs that comprise a number of row (See figure 2A) and a row of keys(See figure 3). One of ordinary skill in the art recognizes that the array having a reduced number of input/outputs comprising combinations may have different number of array.

18 As to claim 9, the array according to claim 8, wherein each set of rows includes a first row (Items 2-6 of figure 4) and a second row (Items 7-9 of figure

4), and the array further comprises at least one passive element positioned between the second row and the array row input/output (Items P0-3 and items 6-9 of figures 4).

19 As to claim 10, the array according to claim 9, further, Thus discloses the passive element is a diode (Items 6-9 of figures 4).

Conclusion

20 The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following cited arts are further to show the sate of art related to keypad array having reduced number of input/outputs and method for generating same.

In the US patent of (6,417,787) Hsu discloses an apparatus and a method for increasing the number of keys in the key-matrix.

21 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sisay Yacob whose telephone number is (571) 272-8562. The examiner can normally be reached on Monday through Friday 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Horabik can be reached on (571) 272-3068. The

fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sisay Yacob

01/20/06

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